

**Notice of References Cited**

Application/Control No.

09/736,294

Applicant(s)/Patent Under  
Reexamination  
MAGGIO ET AL.

Examiner

Harry Vartanian

Art Unit

2634

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2002/0101912 A1	08-2002	Phelts et al.	375/148
	B	US-5,614,855	03-1997	Lee et al.	327/158
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Delay length locked loop in target range tracking Balasubramanian, K. Rajaravivarma, V. Dept. of Comput. Sci. & Eng., Eur. Univ. of Lefke, Mersin, Turkey; This paper appears in: Southeastern Symposium on System Theory, 2001. Proceedings of the 33rd
	V	A semidigital dual delay-locked loop Sidiropoulos, S.; Horowitz, M.A.; Solid-State Circuits, IEEE Journal of , Volume: 32 , Issue: 11 , Nov. 1997; Pages: 1683 - 1692
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.